Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Currently amended) A method in a multi-processor data processing system, having at least one master processor, at least one slave processor, memory, and a system core logic used to interface the processors to the memory, for changing an operating frequency [[for a]] of the system core logic ~~used to interface to memory in the multi-processor data processing system~~, the method comprising:

determining whether the operating frequency of the system core logic should be changed from a ~~default~~ first frequency to ~~another~~ a second frequency;

responsive to determining the operating frequency should be changed, ~~from the default frequency to the another frequency,~~ placing the at least one slave processor ~~processors in the multi-processor data processing system~~ into a non-transactional mode; and

responsive to placing the at least one slave processor into the non-transactional mode, changing the operating frequency [[in]] of the system core logic to the ~~another~~ second frequency.

2. (Currently amended) The method of claim 1 further comprising:

responsive to changing the operating frequency of the system core logic to the second frequency, placing the slave processors into a normal mode.

3. (Currently amended) The method of claim [[2]] 1, wherein the first frequency is a low default frequency, set by a phase locked loop clock in the system core logic, at power on. ~~further comprising:~~

~~completing initialization of the multi-processor data processing system.~~

4. (Currently amended) The method of claim 1, wherein the ~~non-transactional mode is a sleep mode.~~ determining step comprises:

determining, by the master processor, memory speeds of a plurality of memory modules within the memory;

determining a lowest frequency of the memory modules; and

responsive to the lowest frequency being different from the first frequency, determining that the operating frequency of the system core logic should be changed from the first frequency to the second frequency, wherein the second frequency is the lowest frequency.

5. (Currently amended) The method of claim 1, wherein the non-transactional mode comprises one of a sleep mode or [[is]] a mode in which the slave processor ~~processors~~ [[are]] is in a spin loop without generating any external bus transactions to the system core logic.

6. (Currently amended) The method of claim 1, wherein the changing step comprises:

setting a register in the system core logic to a value [[for]] of the ~~another~~ second ~~frequency.~~ frequency;

entering, by the master processor, a delay loop to prevent sending transactions to the system core logic; and

in response to termination of the delay loop, checking, by the master processor, the register in the system core logic to ensure the operating frequency of system core logic has been changed to the second frequency.

7. (Currently amended) The method of claim 1, wherein the determining step, the placing step, and the changing step are performed by [[a]] the master processor in the multi-processor data processing system.

8. (Original) The method of claim 1, wherein the multi-processor data processing system is a symmetric multi-processor data processing system.

9. (Currently amended) A multi-processor data processing system, having at least one master processor, at least one slave processor, memory, and a system core logic used to interface the processors to the memory, for changing an operating frequency [[for a]] of the system core logic ~~used to interface to memory in the multi-processor data processing system~~, the multi-processor data processing system comprising:

determining means for determining whether the operating frequency of the system core logic should be changed from a ~~default~~ first frequency to ~~another~~ a second frequency;

placing means, responsive to determining the operating frequency should be changed ~~from a default frequency to another frequency,~~ for placing the at least one slave processor ~~processors in the multi-processor data processing system~~ into a non-transactional mode; and

changing means, responsive to placing the at least one slave processor into the non-transactional mode, for changing the operating frequency [[in]] of the system core logic to the ~~another~~ second frequency.

10. (Currently amended) The multi-processor data processing system of claim 9, wherein the placing means is the first placing means and further comprising:

second placing means, responsive to changing the operating frequency of the system core logic to the second frequency, for placing the slave processors into a normal mode.

11. (Currently amended) The multi-processor data processing system of claim [[10]] 9, wherein the first frequency is a low default frequency, set by a phase locked loop clock in the system core logic, at power on. ~~further comprising:~~

~~completing means for completing initialization of the multi-processor data processing system.~~

12. (Currently amended) The multi-processor data processing system of claim 9, wherein the ~~non-transactional mode is a sleep mode.~~ determining means comprises:

determining means for determining, by the master processor, memory speeds of a plurality of memory modules within the memory;

determining means for determining a lowest frequency of the memory modules; and

determining means, responsive to the lowest frequency being different from the first frequency, for determining that the operating frequency of the system core logic should be changed from the first frequency to the second frequency, wherein the second frequency is the lowest frequency.

13. (Currently amended) The multi-processor data processing system of claim 9, wherein the non-transactional mode comprises one of a sleep mode or [[is]] a mode in which the slave processor ~~processors~~ [[are]] is in a spin loop without generating any external bus transactions to the system core logic.

14. (Currently amended) The multi-processor data processing system of claim 9, wherein the changing means comprises:

setting means for setting a register in the system core logic to a value [[for]] of the ~~another~~ second ~~frequency.~~ frequency;

entering means for entering, by the master processor, a delay loop to prevent sending transactions to the system core logic; and

checking means, in response to termination of the delay loop, for checking, by the master processor, the register in the system core logic to ensure the operating frequency of system core logic has been changed to the second frequency.

15. (Currently amended) The multi-processor data processing system of claim 9, wherein the determining means, the placing means, and the changing means are located in [[a]] the master processor in the multi-processor data processing system.

16. (Original) The multi-processor data processing system of claim 9, wherein the multi-processor data processing system is a symmetric multi-processor data processing system.

17. (Currently amended) A computer program product in a computer readable medium for a multi-processor data processing system, having at least one master processor, at least one slave processor, memory, and a system core logic used to interface the processors to the memory, for changing an operating frequency [[for a]] of the system core logic ~~used to interface to memory in the multi-processor data processing system~~, the computer program product comprising:

first instructions for determining whether the operating frequency of the system core logic should be changed from a ~~default~~ first frequency to ~~another~~ a second frequency;

second instructions, responsive to determining the operating frequency should be changed, ~~from the default frequency to the another frequency,~~ for placing the at least one slave processor ~~processors in the multi-processor data processing system~~ into a non-transactional mode; and

third instructions, responsive to placing the at least one slave processor into the non-transactional mode, for changing the operating frequency [[in]] of the system core logic to the ~~another~~ second frequency.

18. (Currently amended) The computer program product of claim 17 further comprising:

fourth instructions, responsive to changing the operating frequency of the system core logic to the second frequency, for placing the slave processors into a normal mode.

19. (Currently amended) The computer program product of claim [[18]] 17, wherein the first frequency is a low default frequency, set by a phase locked loop clock in the system core logic, at power on. ~~further comprising:~~

~~fifth instructions for completing initialization of the multi-processor data processing system.~~

20. (Currently amended) The computer program product of claim 17, wherein the ~~non-transactional mode is a sleep mode.~~ first instructions comprises:

first sub-instructions for determining, by the master processor, memory speeds of a plurality of memory modules within the memory;

second sub-instructions for determining a lowest frequency of the memory modules; and

third sub-instructions, responsive to the lowest frequency being different from the first frequency, for determining that the operating frequency of the system core logic should be changed from the first frequency to the second frequency, wherein the second frequency is the lowest frequency.

21. (Currently amended) The computer program product of claim 17, wherein the non-transactional mode comprises one of a sleep mode or [[is]] a mode in which the slave processor ~~processors~~ [[are]] is in a spin loop without generating any external bus transactions to the system core logic.

22. (Currently amended) The computer program product of claim 17, wherein the third instructions comprises:

first sub-instructions for setting a register in the system core logic to a value [[for]] of the ~~another~~ second ~~frequency.~~ frequency;

second sub-instructions for entering, by the master processor, a delay loop to prevent sending transactions to the system core logic; and

third sub-instructions, in response to termination of the delay loop, for checking, by the master processor, the register in the system core logic to ensure the operating frequency of system core logic has been changed to the second frequency.

23. (Currently amended) A data processing system comprising:

a bus system;

a memory connected to the bus system, wherein the memory includes a set of instructions; and

a processing unit connected to the bus system, wherein the processing unit executes a set of instructions to determine whether the operating frequency of a system core logic should be changed from a ~~default~~ first frequency to ~~another~~ a second frequency; place an at least one slave processor ~~processors in the multi-processor data processing system~~ into a non-transactional mode in response to determining the operating frequency should be changed ~~from a default frequency to another frequency~~; and change the operating frequency [[in]] of the system core logic to the ~~another~~ second frequency in response to placing the at least one slave processor into the non-transactional mode.